Debugging USB 2.0 for Compliance: It's Not Just a Digital World

Application Note 1382-3

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Who Should Read This Application Note?

Digital designers developing computer systems and peripherals with USB applications/technology.

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Introduction

It has long been recognized that personal computers (PCs) need to be simpler and easier to use without sacrificing connectivity or expandability. The Universal Serial Bus (USB) was originally developed in 1995 as a low-cost external-expansion bus that makes adding peripherals to a PC as easy as hooking up a telephone to a wall jack. The goal was to create a "Plug and Play" environment. As long as all of the devices adhered to the class definitions then they could be supported by the operating system. The highlights of USB's external-expansion architecture are:

- PC host controller hardware and software
- robust connectors and cable assemblies
- peripheral-friendly master-slave protocols
- multi-port hubs for expandability

Traditionally, peripherals, hubs, and hosts may operate at full speed (12 Mb/s) or low speed (1.5 Mb/s). These speeds are adequate for human-interface devices such as mice or keyboards, but very limiting for next-generation devices such as high-resolution printers and scanners, video-conferencing cameras, and high-density storage devices such as read/write (R/W) DVD drives. High-speed USB is being developed to increase data throughput by a factor of 40 over full speed USB, to a target of 480 Mb/s. The USB 2.0 is a new version incorporating low, full, and high speeds. The USB 2.0 standard is a backward compatible extension of USB 1.1 using the same cables, connectors, and software interfaces, so consumers will see no changes to the usage model.

USB Evolution

A description of the major elements of a USB system (host, hubs, and peripherals) is required to understand the evolution to version 2.0. The USB software in the host PC provides a uniform view of the input/output (I/O) system for the applications software, and manages the dynamic attach and detach of peripherals (called enumeration). During run time the host PC initiates transactions to specific peripherals; each peripheral accepts its transactions and responds accordingly. The host PC software also incorporates the peripheral into the system power management scheme.

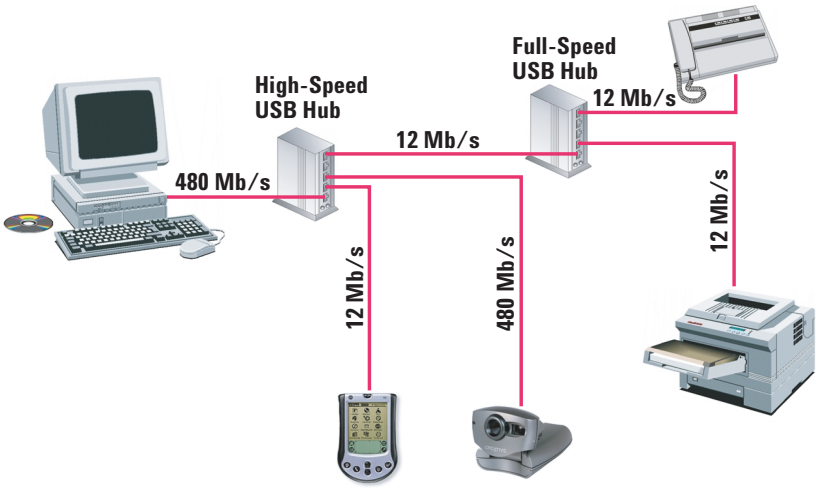

Figure 1. USB systems can manage all three data rates concurrently.

A hub provides additional connectivity for USB peripherals, provides managed power to attached peripherals, and recognizes dynamic attachment of a peripheral. Hubs can be cascaded up to five levels deep. During run time, a hub operates as a bidirectional repeater and repeats USB signals as required on upstream (towards the host) or downstream (towards the peripherals) cables.

All USB peripherals are slaves that obey a defined protocol; they must react to request transactions sent by the host PC. The peripheral sends and receives data to/from the host using a standard USB data format. This standardized data movement to/from the host PC and interpretation by the peripheral give USB its enormous flexibility with little host PC software changes.

USB 2.0 is an evolution of the former USB 1.1 specification, with a higher-performance interface. All three speeds can operate together in a high speed USB system, as shown in figure 1. Today's low/full speed connectors and cables will support the higher speeds of 480 Mb/s without any changes. In this figure, high-speed connections are negotiated between the root hub (in the host PC) and the external high-speed (HS) hub, and between the external HS hub and the video conferencing camera (an HS USB peripheral). All other connections are at full speed USB data rates. The external HS hub is capable of supporting all three data speeds on its downstream ports. Any downstream port of an HS USB hub can support the dynamic attachment of any speed USB device.

High-speed USB data rates permit bandwidth-hungry peripherals to use a USB system, while also creating debugging problems. If only square waves weren't made up of lots of pesky sine waves, then the world would be truly digital, and life would be simple. Back in the good old days of low speed USB, signaling rates were merely 1.5 Mb/s. Now, with the analog effects of the high-speed data rates (480 Mb/s), radio frequency (RF) and even microwave design techniques must be used. Signal integrity becomes a critical part of every design. However, the digital world, or "data domain", also creates issues that affect the designer: interaction of devices, multi-speed traffic, and large amounts of data. Because the analog and digital behaviors are interrelated, designers of high-speed USB devices need to take a holistic approach to debugging, validating, and characterizing their designs.

The first step in the testing process is the initial turn-on of the hardware—looking with an oscilloscope at fundamental analog signals being transmitted and received. Key analog measurements need to be reviewed and are ultimately required for compliance testing. The USB 2.0 measurement suite includes signal integrity, in-rush current, drop, droop, and many more.

Signal Integrity is Critical

The first hardware test is to look at the D+ and D- lines with an oscilloscope, as shown in figure 2, to verify that they meet the USB Implementers' Forum (USB-IF) electrical test specification. These test requirements can be met using an oscilloscope and then running *The MathWorks* MATLAB® analysis software with the USB-IF test scripts. The goal of this measurement series is to test signal quality (including such parameters as EOP (end-of-packet) width, measured signaling rate, crossover voltage range, and jitter), as well as the data signal eye to verify that the data fits the specified eye-diagram parameters.

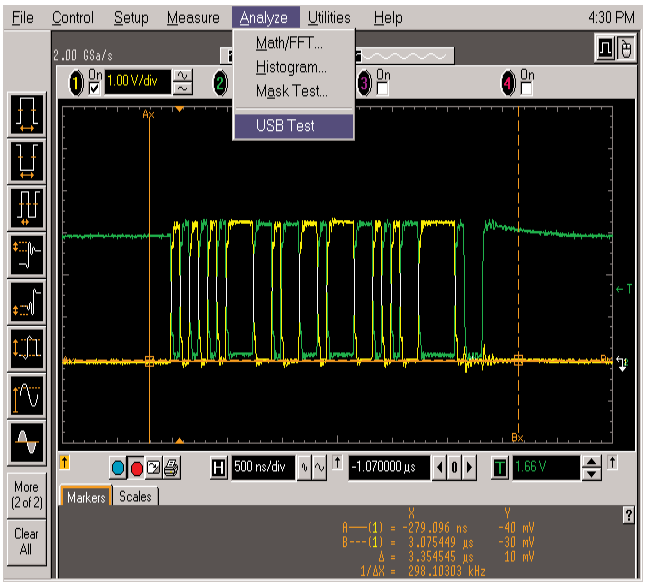

Figure 2. D+ and D- data signals are automatically bracketed by the Agilent Infiniium 54800 Series USB test option.

Agilent Infiniium 54800 Series oscilloscopes, along with Agilent probes and test fixtures, or "breakout boards", are crucial for replicating the USB-IF compliance tests. The Infiniium USB test option (Agilent part number B30 or E2645A) makes USB signal integrity pre-compliance testing as simple as making an automatic measurement. Infiniium has significantly reduced the work associated with USB testing by eliminating the need to manually transfer oscilloscope data to another PC for analysis. The Infiniium USB test option features a run-time version of MATLAB embedded in the scope for use with the USB-IF test scripts—a one-box solution that speeds signal quality testing. Figure 3 shows an eye-diagram measurement generated by the Agilent Infiniium 54800 Series oscilloscope, using the internal run-time MATLAB software.

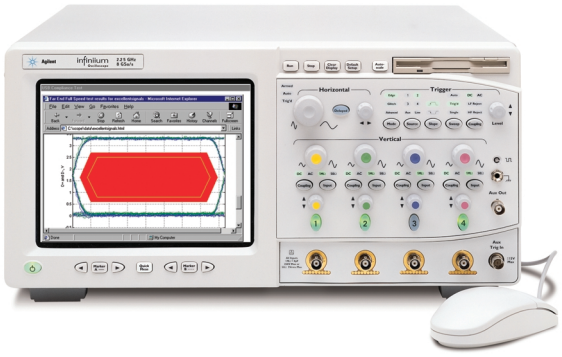

Figure 3. Including MATLAB within the Agilent Infiniium 54800 Series oscilloscopes simplifies USB measurements.

Failures at this stage can be caused by a variety of conditions. Failure to meet the upper and/or lower voltage levels is typically caused by improper termination. Reduction or collapse of the data eye is often caused by jitter. A common source of jitter is noise from the clock or from the power supply, but there are many other sources that also must be considered.

Attention To Detail Prevents Current Violations

Another analog concern that requires detailed attention is current measurement. Whether a device is self-powered or bus-powered, there are numerous combinations of current conditions. USB 2.0 designers need to measure current draws from hot-plug conditions, low-power states, suspend states, and other conditions. The operating current draw and suspend current draw are DC current values that can be measured with a simple DC ammeter. The transient current measurements, such as hot-plug in-rush current and peak operating current, require an oscilloscope and a current probe. The dynamic nature of many of the current specifications makes this the only possible way to acquire these measurements. An Agilent Infiniium 54800 Series oscilloscope with an 1147A current probe is capable of capturing these transient current events. The triggering capabilities of a scope may also be necessary to measure the bus at a specific instant in time. Figure 4 shows peak and average current measurements on an oscilloscope. Peak and average power values can be computed by the oscilloscope's software using these measured current values.

The most common types of current specification failures occur when the maximum current draw is exceeded, which typically happens during a hot-plug condition. When trying to meet the suspend-current requirements, attention to detail is required to ensure that everything possible in the circuit is turned off. For a self-powered device, the +5 V_{dc} and V_{bus} must be completely isolated from each other.

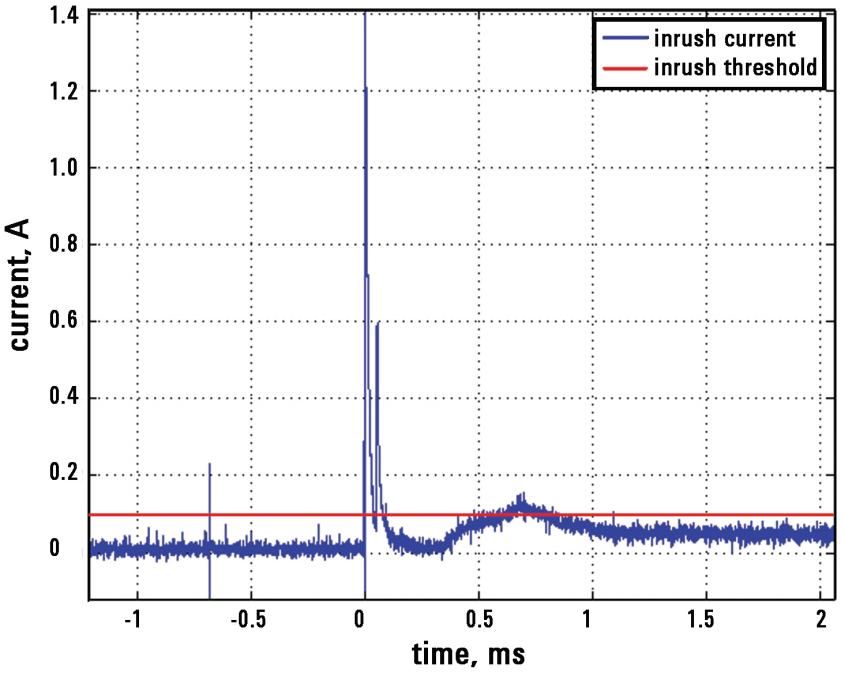

Figure 4. Peak and average current values as measured by an oscilloscope.

Verification of Data Integrity

Once it has met USB 2.0 voltage, signal integrity, and current requirements, the DUT is likely to be a good bus citizen at the physical level. However, the challenge is just starting; the device must now be tested for compliance with the Universal Serial Bus Implementers' Forum (USB-IF) interoperability specification. Any peripheral device on the bus must be able to communicate with its hub. The hubs must be able to communicate with the host, each other, and up to seven peripherals, while handling all three data transfer rates plus isochronous and bulk data transfers.

A USB system is a form of network with a wide variety of interdependencies, so determining the cause of a data error or a performance problem can be very difficult. A logic analyzer lets you see data traffic, make critical timing measurements, and verify protocols, making it the best tool for detecting and debugging higher-level problems such as enumeration failure or corrupted data packets. Deep acquisition memory and powerful real-time triggering provide a quick and reliable method of capturing elusive problems.

In figure 5, the logic analyzer protocol (or transaction) listing shows that the logic analyzer triggered on a cycle redundancy check (CRC) error. Because of the logic analyzer's deep acquisition memory, the designer can see the events that led up to the failure (pre-trigger events) and how the device responded to this error condition (post-trigger events). The ability to turn off input and/or output negative acknowledge characters (NAKs) allows more efficient use of memory and saves the user from having to wade through information that may not be useful.

Being able to measure time relationships between events, like a request and an acknowledge, is an important tool for debugging a wide variety of problems. This measurement methodology is commonly referred to as event timing. Logic analyzers and other types of protocol tools do have the ability to provide event timing through the use of time stamp. A time stamp is simply a counter that keeps track of the time between each state event. This key feature has always been a part of logic analyzers and provides event timing with accuracy to 4 ns.

If accuracy greater than 4 ns is needed or if true asynchronous timing is required, then a scope should be connected to the D+ and D- lines or to the output of the transceiver interface chip.

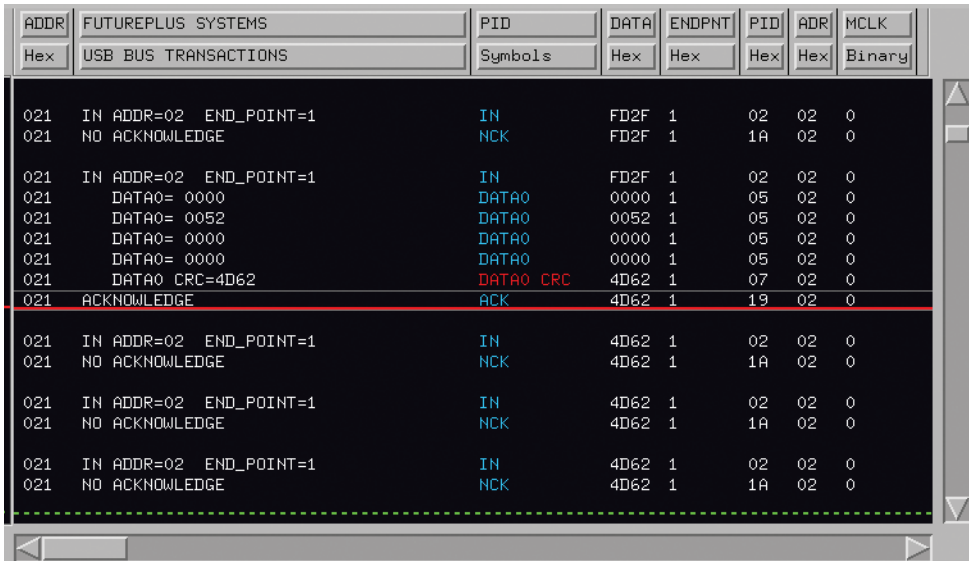

Figure 5. Logic analyzer protocol listing shows a trigger on a CRC error.

Integration of Tools Equals Simplification

A wide variety of tools are needed to make accurate analog scope measurements, current measurements, and to capture and analyze data. The complexities of oscilloscopes, MATLAB software, logic analyzers, and breakout boards turn debugging, performance characterization, and specification compliance testing into daunting tasks. Fortunately, there are tools available to USB 2.0 designers that simplify the process by taking advantage of the integration of PCs and test equipment. For example, MATLAB software is integrated into the Agilent Infiniium 54800 Series oscilloscopes, eliminating the need to make a measurement and then transfer the data to a PC to do the analysis. Now all of these steps can be performed as a single measurement step. The same is true for current measurements using the oscilloscope. Today's logic analyzers and oscilloscopes are integrated so that cross-triggering and even sharing of data on a single display simplify the debug process.

Another key test and debug technique now available is cross-bus analysis. To determine the root cause of a problem, it may be necessary to simultaneously and separately measure the input and output of a hub or hubs, to study a hub and the PCI bus on a USB/PCI adapter card, or to observe the interaction between the USB, PCI, and PC memory system. Logic analyzers are capable of looking at multiple buses simultaneously, having one bus trigger other buses, and having all of the time-correlated data presented on a single display.

USB 2.0 is a fast, reliable bus architecture that improves the usefulness and capabilities of the PC world. However, it is not a slow, simple digital bus: It is complex and sophisticated, and requires designers to exercise their skill and talent. By following the guidelines and advice set forth by the USB-IF and using tools designed for the high-speed analog/digital world, you can develop reliable USB 2.0 products and quickly bring them to the marketplace.

Analysis Probe for USB 1.1 and 2.0

The FS 4120 USB analysis probe from FuturePlus Systems Corporation (Agilent part number FSI-60050), when combined with the Agilent Technologies 16700 Series logic analysis systems and Infiniium 54800 Series oscilloscopes, provides engineers with complete system debugging, verification, and compliance testing of USB 2.0 peripherals, hubs, and USB-based systems.

The FS 4120 probe provides an electrical and mechanical interface for passive bus analysis between a USB DUT and Agilent logic analyzers. It has test points for DC current, in-rush current, and suspend current measurements for bus-powered devices. SMA connectors and hardware-assisted oscilloscope triggering are provided for easy oscilloscope triggering and measurements. Key features of the new probe include:

- complete USB serial-to-parallel decoding, providing a protocol-level view of bus traffic
- dual-bus operation with time-correlated displays for hub debug
- support for current measurements on bus powered devices, including in-rush current
- external power supply connection for USB devices
- error detection, including bad PID, invalid PID, serial bit stuffed, CRC, Start of Frame, USB reset, and USB bus communication errors
- operation at all USB speeds: 480 Mb/s, 12 Mb/s, and 1.5 MB/s
- support for all types of data transfers, including isochronous transfers
- LEDs that provide quick visual identification of bus status and activity
- SMA connections for easy triggering and connection to a high-speed oscilloscope
- Input/Output - NAK suppression (FS/HS) capability

Powerful triggering can be set up on any address, end point, data pattern, data CRC, or USB error. All USB cycles and transaction identifiers are decoded by protocol-sensitive clocking logic. Packet identifiers enable users to store all USB traffic, store only certain packet types, or store only packets to/from a user-specified function. The included software provides a complete color-coded transaction and packet level decode of all the USB traffic.

The FS 4120 has two independent USB and analyzer interfaces. This unique feature enables the designer to independently measure a high-speed device and a full-speed device at the same time, without having to purchase a second analysis probe.

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Related Literature

Publication Title	Publication Type	Publication Number
Agilent Technologies 16700 Series Logic Analysis System	Product overview	5968-9661E
Agilent Infiniium 54800 Series Oscilloscopes	Color brochure	5980-2388EN/EUS
Agilent Infiniium 54800 Series Oscilloscopes	Product overview	5980-2397EN/EUS

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